INL/EXP-20-59298-Revision-0

PosterExpo_AshleyRivera_2020

August 2020

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Prepared for the
U.S. Department of Energy
Under DOE Idaho Operations Office
Contract DE-AC07-05ID14517

www.inl.gov
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Increasing the SATS Uncertainty Safety Margin

All values are uncertainties(±) in mVdc

Definitions

- PPS: Plant Protection System: Monitors conditions in the nuclear reactor and scrams the reactor (initiates automatic shutdown) if dangerous conditions occur.
  (Ex: reactor temperatures, pressures, neutron levels)
- SATS: Surveillance And Test System: Tests the functionality of the Plant Protection System (PPS).
- DAC and ADC: Digital-to-Analogue Converter and Analogue-to-Digital Converter

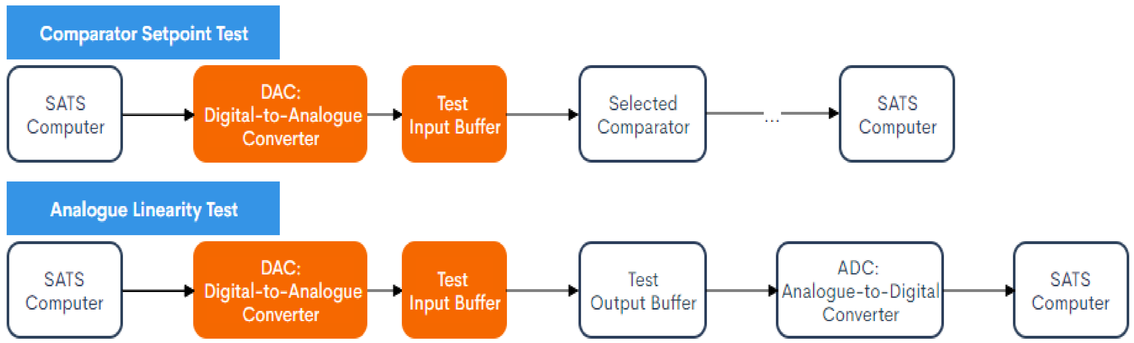
Background

- Comparators: A component of PPS. Takes an input signal from a detector in the reactor and compares it to a safety setpoint. If the signal from the detector is above the setpoint, the comparator sends a trip signal alerting that something is wrong.
- Comparator Setpoint Test: The SATS computer sends signals to the DAC to the Test Input Buffer to the selected comparator to see if it trips, overriding the comparator's usual input from a detector. This checks if the trip point has drifted away from the setpoint value.
- Analogue Linearity Test: A SATS self-check test. The SATS computer sends a signal to the DAC and input buffer, however, instead of sending it to a comparator, it sends it to the Test Output Buffer, then to the ADC. This tests checks whether the ADC, DAC, and test buffers are calibrated properly.

Project

A recalibration will only be done if the signal sent and received by the Analogue Linearity Test is more than ±61 mVdc of the expected value.

This project analyzes whether this accuracy range can be increased without impacting the uncertainty analysis of the Comparator Setpoint Test.



Equations

- Eq 1. is the total uncertainty of the Comparator Setpoint Test. This must be under **±101 mVdc**. The max allowed comparator uncertainty is ±70 mVdc. This means that the combined DAC and Input Buffer must be less than **±72.8 mVdc**.

$$Eq.1 \qquad \sqrt{(DAC + Buffer_{in})^2 + (Comparator)^2} = Comparator\ Setpoint\ Uncertainty$$

$$Calibrated\ Values: \quad \sqrt{(\pm 5)^2 + (\pm 70)^2} = \pm 70.2\ mVdc$$

$$Max\ Allowed\ Uncertainty: \quad \sqrt{(\pm \mathbf{72.8})^2 + (\pm 70)^2} = \pm 101\ mVdc$$

- Eq. 2 is the total uncertainty for the Analogue Linearity Test. If these are all calibrated, the result is ±12.3 mVdc. **Currently, this test will fail if the result is ±61 mVdc.** Based on Eq. 1, it **MUST FAIL** before the DAC and Input Buffer drift passes **±72.8**

$$Eq.2 \qquad \sqrt{ADC^2 + (DAC + Buffer_{in})^2 + {Buffer_{Out}}^2} = Analogue\ Linearity\ Uncertainty$$

$$Calibrated\ Values: \quad \sqrt{(\pm 5)^2 + (\pm 5)^2 + (\pm 10)^2} = \pm 12.3\ mVdc$$

Scenario Calculations

Scenario A:				Scenario B:			
ADC	DAC+Input Buffer	Output Buffer	Total Uncertainty	ADC	DAC+Input Buffer	Output Buffer	Total Uncertainty
12.3	5	10	**16.62**	12.3	5	10	**16.62**
12.3	6.25	10	**17.04**	15.375	6.25	12.5	**20.78**
12.3	7.5	10	**17.54**	18.45	7.5	15	**24.93**
...	...	...	...	...	...	...	...
12.3	17.5	10	**23.61**	43.05	17.5	35	**58.18**
12.3	18.75	10	**24.55**	46.125	18.75	37.5	62.33
12.3	20	10	**25.52**	49.2	20	40	66.49
...	...	...	...	...	...	...	...
12.3	58.75	10	**60.85**	12.3	58.75	10	**60.85**
12.3	60	10	62.06	147.6	60	120	199.46
12.3	61.25	10	63.27	150.675	61.25	122.5	203.62
...	...	...	...	...	...	...	...
12.3	71.25	10	72.99	175.275	71.25	142.5	236.86
12.3	72.5	10	74.21	178.35	72.5	145	241.02
12.3	73.75	10	75.43	181.425	73.75	147.5	245.17
12.3	75	10	76.66	184.5	75	150	249.33
12.3	76.25	10	77.88	187.575	76.25	152.5	253.49

Results

Data is provided for two scenarios:

Scenario A is a worse-case scenario where only the DAC and Input Buffer drift. In this case, the Analogue Linearity Test needs to fail at **±74 mVdc.**

Scenario B is a more optimistic scenario where all measurements drift by the same percentage. In this case, the Analogue Linearity Test needs to fail at **±241 mVdc**.

Significance of Results

This project establishes the **margin of safety** that the SATS Analogue Linearity Test can pass before it needs to fail to catch an error. Currently, the test must be accurate to ±61 mVdc to pass. According to these results, this **could be increased to ±74 mVdc** and still catch when the DAC and Input Buffer go dangerously out of calibration, even in a worse-case scenario. The acceptable uncertainty could be increased even more and still have a high probability of catching the DAC before it drifts too far.

Should this test ever need to be altered, this safety margin will help determine if the tests will still meet required safety standards.